

It will be appreciated that the circuits illustrated in FIG. 5 for next bit generator 404 and sequence generator 408 may be replaced with other circuits as is generally known in the art to achieve the same function as pattern generator 500. Additionally, the circuits illustrated in FIG. 5 may be altered as generally known in the art to respond to other ranges of numbers described in this application.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

What is claimed is:

1. A method for generating a serial pattern comprising a first plurality of bits, the method comprising the steps of:
 - (A) generating a second plurality of bits having a first value and a least significant bit, wherein the second plurality of bits includes less bits than the first plurality of bits;
 - (B) comparing the first value with at least one number;
 - (C) if the first value is equal to the at least one number, then generating a next bit in the serial pattern having a same state as the least significant bit in the second plurality of bits; and
 - (D) if the first value is not equal to the at least one number, then generating the next bit in the serial pattern having a complement state of the least significant bit in the second plurality of bits.

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2. The method of Claim 1, further comprising the steps of:

(E) shifting the second plurality of bits, wherein the second plurality of bits has a second value; and

(F) loading the least significant bit with the next bit.

3. The method of Claim 1, wherein step (C) comprises generating the next bit in the serial pattern having the same state as the least significant bit in the second plurality of bits if the first value is not equal to the at least one number, and wherein step (D) comprises generating the next bit in the serial pattern having the complement state as the least significant bit in the second plurality of bits if the first value is equal to the at least one number.

4. The method of Claim 1, wherein the second plurality of bits comprises n bits, and the at least one number comprises one through 2^{n-1} inclusive.

5. The method of Claim 1, wherein the second plurality of bits comprises n bits, and the at least one number comprises $2^{n-1} - 1$ through $2^n - 2$ inclusive.

6. A pattern generator comprising:

a sequence generator outputting a serial sequence of bits and a plurality of bits having a value;

a comparator coupled to the sequence generator, the comparator receiving the plurality of bits and at least one number, wherein the comparator compares the value with the at least one number and generates a comparison result; and

a next bit generator coupled to the comparator and the sequence generator, wherein the next bit generator receives the comparison result and one of the plurality of bits, and wherein the next bit generator generates a next bit for the serial sequence of bits.

(D) if the first value is not equal to the at least one number, then generate the next bit in the pattern having a complement state of the least significant bit in the second plurality of bits.

18. The medium of Claim 17, wherein the sequence of instructions further causes the digital signal processing device to:

(E) shift the second plurality of bits, wherein the second plurality of bits have a second value; and

(F) load the least significant bit with the next bit.

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